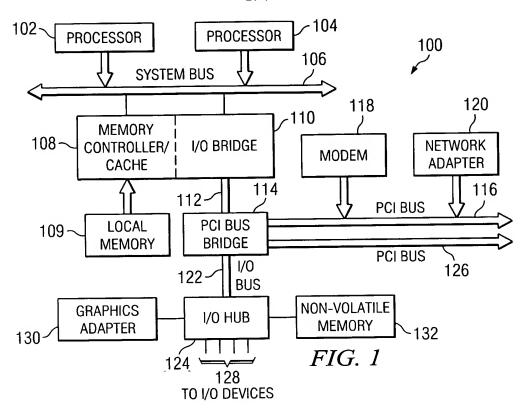
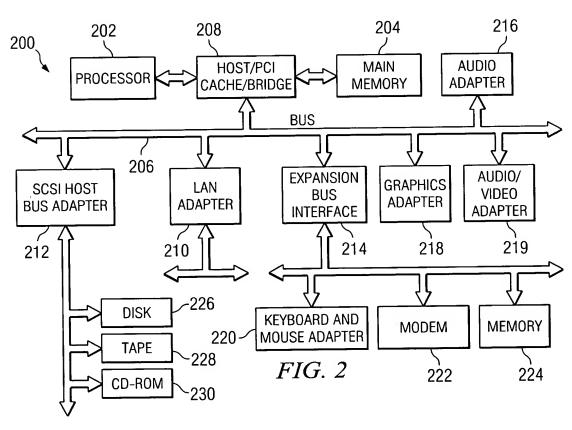
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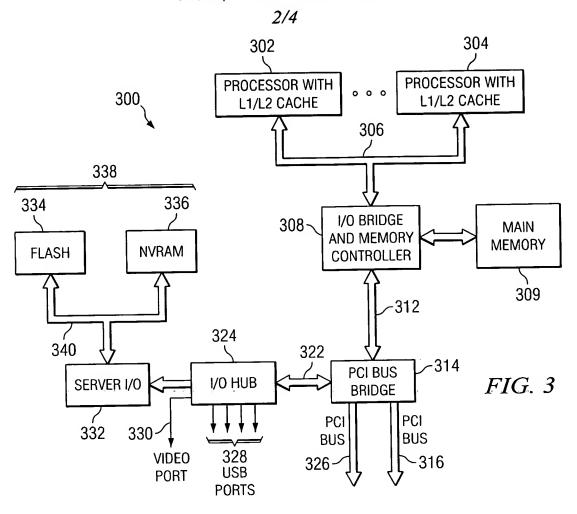


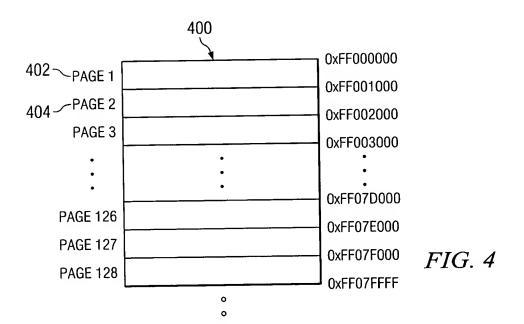




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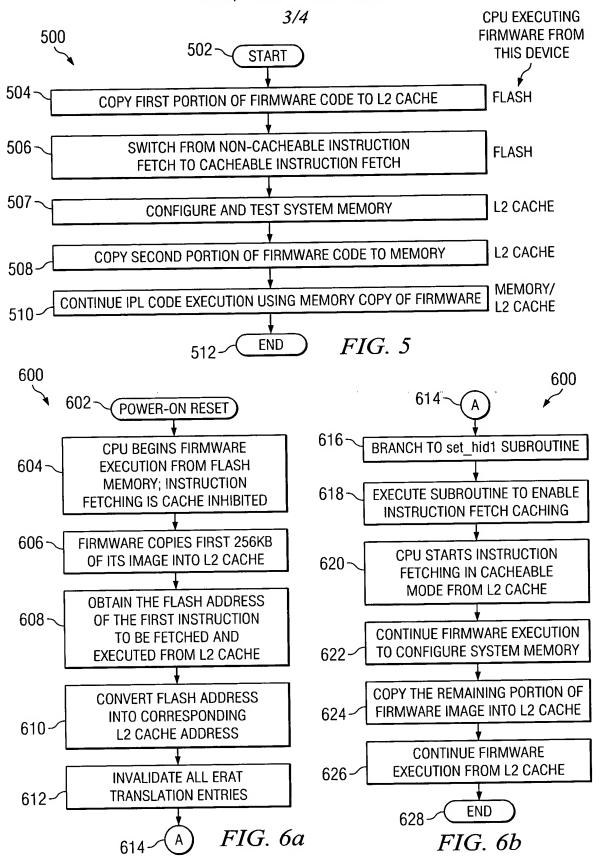
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R5 has L2 address of go_to_cache routine 4/4 Routine to copy firmware code from flash into L2 cache # Convert flash addr in r5 $\# R9 = 0 \times D0 D0 00 00 00$ # R3 = 0xFF000000 FF005014] bne copy_first_256k_flash_image FF005028] addi r5,r5,(go to cache-this addr) # into L2 address [FF005000] bi read_128_bytes_from_flash [FF005004] bi write_128_byte_to_L2_cache [00D05050] :ori r0,r0,0 #noop FF005010] addic. r10,r10,-128 mtspr SRR0,r5 After executing set_hid1 subroutine to enable instruction fetch cacheable FF00501C] mtspr SRR1,r4 FF00502C] addis r3,r3,-4 FF00500C] addi r3,r3,128 FF005008] addi r9,r9,128 [FF005020] bi this addr FF005030] addis r9,r9,-4 mfspr r8,HID1 FF00504C] b set_hid1 FF005034] subf r5,r3,r5 FF005038] add r5,r5,r9 FF005044] or r8,r8,r7 FF005018] mfmsr r4 copy first 256k flash image: [FF005024] mflr r5 FF005048] sibia Starting at 0xFF000100 from reset_interrupt_handler Cacheable instruction fetch continues at 0x00D05050 [00D05054] FF00503C] FF005040] to_cache: this addr: Instruction Address Flow ള FF000110] addi r3,r3,(flash_begin - this_flash_addr) # R3 = 0xFF000000# R7 = 0x00200000000000000# R10 = 0x0D040000 = 256K # R9 = 0x00000000 = 13MFirst two pages of the firmware image in flash FF00011C] b copy_first_256k_flash_image [FF000104] addis r10,r0,0x0004 [FF000100] addis r9,r0,0x00D0 [FF000108] bl this_flash_addr FF000118] ridicl r7,r7,53,0 [FF000FF4] mtspr HID1, r8 FF000FF8] mtspr HID1, r8 FF000114] addi r7,r0,1 Appendix A [FF001FFC] .long 0 FF001000] .long 0 [FF00010C] mtr r3 FF000FFC] rfid reset_interrupt_handler: [FF000000] [FF000004] FF001004 [FF000120] flash addr: flash_begin: set hid1: ▲